What is Claimed is:

1. An inverter, comprising:

a transformer;

a first switch transistor with one of the source/drain thereof electrically coupled to the primary side of said transformer;

a second switch transistor with one of the source/drain thereof electrically coupled to the primary side of said transformer;

a reset capacitor electrically coupled between the other of the source/drain of said first switch transistor and the other of the source/drain of said second switch transistor; and

a control circuit for generating two switch control signals in response to a voltage feedback signal representing the current value at the secondary side of said transformer and respectively outputting to the gate of said first switch transistor and the gate of said second switch transistor to thereby cause said first switch transistor and said second switch transistor not to conduct current at the same time.

2. The inverter of claim 1, further comprising:

a first snubber capacitor electrically coupled between the source and the drain of said first switch transistor; and

a second snubber capacitor electrically coupled between the source and the drain of said second switch transistor.

3. The inverter of claim 1, further comprising a decoupling capacitor electrically coupled to the secondary side of said transformer.

4. The inverter of claim 1, wherein said control circuit comprises a driving circuit which utilizes the voltage across said reset capacitor as driving power for generating said two switch control signals.

5. The inverter of claim 1, wherein said control circuit comprises:

an error amplifier, for sensing said voltage feedback signal representing the current value at the secondary side of said transformer

and a reference voltage to perform an error amplification; and

a pair of comparators for generating said two switch control signals according to the comparison result of the output of said error amplifier and a reference triangular wave.

6. The inverter of claim 5, wherein said control circuit further comprises a driving circuit for enhancing the driving power of said two switch control signals.

7. The inverter of claim 5, wherein said control circuit further controls the current value at the secondary side of said transformer according to a burst mode control signal received by said error amplifier.

8. The inverter of claim 5, wherein said pair of comparators comprise:

a voltage-dividing resistor electrically coupled to the output terminal of said error amplifier for providing two outputs with different voltages;

a first comparator electrically coupled to one of the two outputs of said voltage-dividing resistor for generating one of said two switch control signals; and

a second comparator electrically coupled to the other of the two outputs of said voltage-dividing resistor for generating the other of said two switch control signals.

9. The inverter of claim 1, wherein said control circuit further controls the current value at the secondary side of said transformer according to a burst mode control signal.

10. The inverter of claim 1, wherein said control circuit further renders both said first and said second switch transistors non-conducting during the interval between the conducting of said first switch transistor and the conducting of said second switch transistor.

11. A lamp ignition system, comprising:

a discharge lamp; and

an inverter;

wherein said inverter comprising:

a transformer with the secondary side thereof electrically coupled to said discharge lamp;

a first switch transistor with one of the source/drain thereof electrically coupled to the primary side of said transformer;

a second switch transistor with one of the source/drain thereof electrically coupled to the primary side of said transformer;

a reset capacitor electrically coupled between the other of the source/drain of said first switch transistor and the other of the source/drain of said second switch transistor; and

a control circuit for generating two switch control signals in response to a voltage feedback signal representing the current value at the secondary side of said transformer and respectively outputting to the gate of said first switch transistor and the gate of said second switch transistor to thereby cause said first switch transistor and said second switch transistor not to conduct current at the same time.

12. The lamp ignition system of claim 11, wherein said inverter further comprises:

a first snubber capacitor electrically coupled between the source and the drain of said first switch transistor; and

a second snubber capacitor electrically coupled between the source and the drain of said second switch transistor.

13. The lamp ignition system of claim 11, wherein said inverter further comprises a decoupling capacitor electrically coupled between the secondary side of said transformer and said discharge lamp.

14. The lamp ignition system of claim 11, wherein said control circuit comprises a driving circuit which utilizes the voltage across said reset capacitor as driving power for generating said two switch control signals.

15. The lamp ignition system of claim 11, wherein said control circuit comprises:

an error amplifier for sensing said voltage feedback signal representing the current value through said discharge and a reference voltage to perform an error amplification; and

a pair of comparators for generating said two switch control signals according to the comparison result of the output of said error amplifier and a reference triangular wave.

16. The lamp ignition system of claim 15, wherein said control circuit further comprises a driving circuit for enhancing the driving power of said two switch control signals.

17. The lamp ignition system of claim 15, wherein said control circuit further controls the current value through said discharge lamp according to a burst mode control signal received by said error amplifier.

18. The lamp ignition system of claim 11, wherein said control circuit further controls the current value through said discharge lamp according to a burst mode control signal.

19. An inverter, comprising:

a transformer;

a first switch transistor with one of the source/drain thereof electrically coupled to the primary side of said transformer;

a second switch transistor with one of the source/drain thereof electrically coupled to the primary side of said transformer;

a reset capacitor electrically coupled between the other of the source/drain of said first switch transistor and the other of the source/drain of said second switch transistor; and

a control circuit for controlling said first switch transistor and said second switch transistor not to conduct current at the same time.

20. The inverter of claim 19, wherein said control circuit comprises

a driving circuit which utilizes the voltage across said reset capacitor as driving power for generating said two switch control signals respectively output to said first switch transistor and said second switch transistor so as to reduce the conducting resistance thereof.

21. The inverter of claim 19, wherein said control circuit further renders both said first and said second switch transistors non-conducting during the interval between the conducting of said first switch transistor and the conducting of said second switch transistor.

22. The inverter of claim 19, further comprising:

a first snubber capacitor electrically coupled between the source and the drain of said first switch transistor; and

a second snubber capacitor electrically coupled between the source and the drain of said second switch transistor.